Intel® BSDL Validation on a 31154 133MHz PCI Bridge

Application Note

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1.0 Introduction

This application note describes the Intel® Boundary Scan Description Language (BSDL) syntax, semantics, and hardware test validation and results on a 31154 133MHz PCI Bridge.

2.0 BSDL Syntax & Semantics

BSDL syntax and semantics software has been run against the BSDL listed below. No syntax and semantics software violations were found:

```
i31154_A0R1
```

Note: _A0 indicates silicon Rev A0 was used for testing; R1 indicates first BSDL release

3.0 BSDL Hardware Validation

The test validation test was performed on the BSDLWorks™ Test Fixture. Test software was a ScanWorks 3.3 project utilizing four test actions. The 31154 device **passed** all tests run as described in Section 3.1.3.

3.1 BSDL Hardware Test Validation Detail

This section details the results of the ScanWorks 3.3 boundary scan validation of BGA package type. Three (3) devices were used in the Validation.

3.1.1 Materials Used

The following materials were used during testing:

- Adaptor 1163
- BSDL file: i31154_A0R1
- ScanWorks Intel® 31154 133MHz PCI Bridge Project
- Three devices that were unmarked

3.1.2 Tests Performed

The following four tests were performed on the three test devices:

- Data Register Test
  Scan Path ATPG uses only Data Register (DR) scans on the bypass registers or, if present, the IDCODE registers of the boundary-scan devices. No Instruction Register (IR) scans are used in this test to prevent possible damage to the design from passing harmful values. The design being tested is left in the functional mode. For devices with secondary scan paths, only the default scan path is validated.

- Instruction Register Test

  Instruction Register (IR) Verify performs an IR Scan on the target design and checks the outputs of the instruction registers of each device from TDO to TDI.

  If 01 is the first two bits received from each device instruction register, the design being tested passes the test. Each IR Scan ends in Test-Logic-Reset state to minimize the possibility of damage to hardware.

- Scan Path Verify Test
  - Chain - checks the TDI, TDO, TMS, and TCK signals in your boundary-scan chain. If this test fails, no other tests are run
  - Chain Length - checks the length of the boundary-scan register for each device in the boundary-scan path.
  - ID Code - tests all components that have an ID code register. This verifies that the devices with ID codes match those defined in your BSDL description, in the order described in the scan path.
  - Usercode – tests all components that have a usercode register. This verifies that the devices with usercodes match those defined in your BSDL description.
  - IR Capture - checks the instruction register capture value for all components in the selected chain. This verifies that the instruction register for each device is functioning correctly.
  - TRST Test - Test the proper functioning of the TRST of the devices that implement TRST, one at a time
- Interconnect Test

  Boundary-scan interconnect tests provide 100% pin-level fault coverage for stuck-at conditions, shorts, and opens on pure boundary-scan nets. The interconnect tests concentrate on maximizing your fault coverage while maintaining safe testing conditions.

3.1.3 Tests Conditions

The following test conditions were observed:

- VCCP, P_VIO, S_VIO: 3.3V +/- 5%
- VCC, S_VCCA, P_VCCA: 1.3V +/- 1%

Summary: All devices passed the tests listed in Table 1.

Table 1. Test Results by Test Type (3 chips tested per type)

Test	Mode	Result
Data Register	Test 8Mhz Clock (Mode Free Run)	Passed
Instruction Register Test	8Mhz Clock (Mode Free Run)	Passed
Scan Path Verify Test	8Mhz Clock (Mode Free Run)	Passed
Interconnect Test	8Mhz Clock (Mode Free Run)	Passed
Data Register Test	8Mhz Clock (Mode Gated)	Passed
Instruction Register Test	8Mhz Clock (Mode Gated)	Passed
Scan Path Verify Test	8Mhz Clock (Mode Gated)	Passed
Interconnect Test	8Mhz Clock (Mode Gated)	Passed

4.0 Findings

The following list describes test findings:

- Linkage bit R_REF pin E5 had no effect on test results if floated, pulled high or low.
- Scan input only SCAN_EN pin C1 performed as modeled in the BSDL during all tests. Constraining this pin high or low did not effect any other scan operation during test.
- Linkage bit S_PCIXCAP pin R23 was left floating during all testing since this signal was noted as analog.

5.0 Non-Standard Efforts

None

6.0 Summary and Recommendations

This device does not utilize compliancy pins and no compliance issues occurred during testing. All devices were successfully tested with no recommendations needed.